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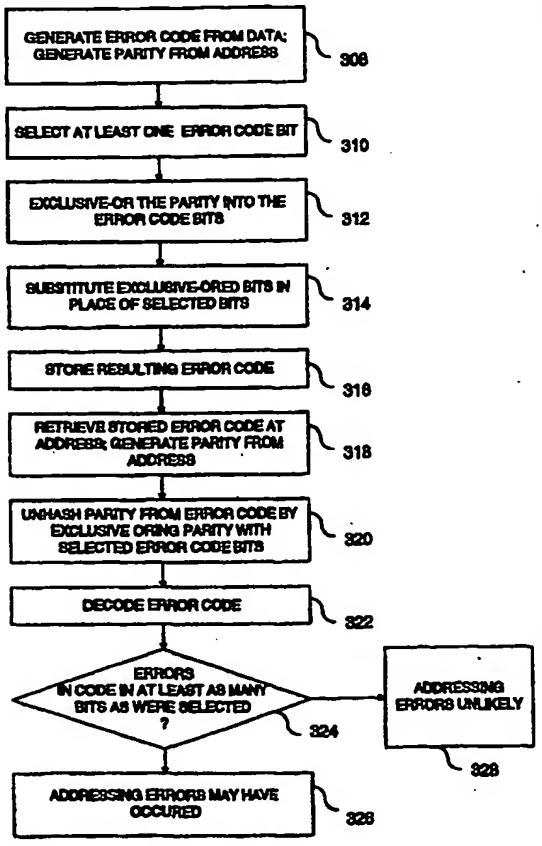
(54) Title: METHOD AND APPARATUS FOR DETECTING MEMORY ADDRESSING ERRORS

(57) Abstract

A method and apparatus allows for detection of addressing errors in an addressable memory device. Data bits may be transformed into an error code such as a Hamming code. Address parity is hashed into selected error code bits, and the result is stored. Upon retrieval, address parity is generated, and unhashed from the retrieved data, and the result is checked for errors, for example using conventional Hamming techniques. Address errors appear as data errors, allowing for detection of data and address errors using a single detector.



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METHOD AND APPARATUS FOR DETECTING MEMORY ADDRESSING ERRORS

Field of Invention

This invention relates to digital storage systems, and specifically to error detection capabilities in an addressable, digital memory system.

Related Applications

The subject matter of this application is related to the following applications:

application serial number _____ entitled "Method, System and Apparatus for Detecting Duplicate Entries in a Look-Up Table" filed on June 9, 1995 by Nirmal R. Saxena;

application serial number _____ entitled "Method, System and Apparatus for Efficiently Generating Binary Numbers for Testing Storage Devices" filed on June 9, 1995 by Nirmal R. Saxena;

application Serial Number _____ entitled "METHOD AND APPARATUS FOR ROTATING ACTIVE INSTRUCTIONS IN A PARALLEL DATA PROCESSOR" filed on June 1, 1995 by Sunil Savkar, Michael C. Shebanow, Gene W. Shen, and Farnad Sajjadian;

application Serial Number _____ entitled "PROGRAMMABLE INSTRUCTION TRAP SYSTEM AND METHOD" filed on June 1, 1995 by Sunil Savkar, Gene W. Shen, Farnad Sajjadian, and Michael C. Shebanow;

application Serial Number 08/388,602 entitled "INSTRUCTION FLOW CONTROL CIRCUIT FOR SUPERSCALER MICROPROCESSOR" filed on February 14, 1995 by Takeshi Kitahara;

application Serial Number 08/388,389 entitled "ADDRESSING METHOD FOR EXECUTING LOAD INSTRUCTIONS OUT OF ORDER WITH RESPECT TO STORE INSTRUCTIONS" filed on February 14, 1995 by Michael A. Simone and Michael C. Shebanow;

application Serial Number 08/388,606 entitled "METHOD AND APPARATUS FOR EFFICIENTLY WRITING RESULTS TO RENAMED REGISTERS" filed on February 14, 1995 by DeForest W. Tovey, Michael C. Shebanow and John Gmuender;

application Serial Number 08/388,364 entitled "METHOD AND APPARATUS FOR COORDINATING THE USE OF PHYSICAL REGISTERS IN A MICROPROCESSOR" filed on February 14, 1995 by DeForest W. Tovey, Michael C. Shebanow and John Gmuender;

application Serial Number 08/390,885 entitled "PROCESSOR STRUCTURE AND METHOD FOR TRACKING INSTRUCTION STATUS TO MAINTAIN PRECISE STATE" filed on February 14, 1995 by Gene W. Shen, John Szeto, Niteen A. Patkar and Michael C. Shebanow;

application Serial Number 08/397,810 entitled "PARALLEL ACCESS MICRO-TLB TO SPEED UP ADDRESS TRANSLATION" filed on March 3, 1995 by Chih-Wei David Chang, Kioumars Dawallu, Joel F. Boney, Ming-Ying Li and Jen-Hong Charles Chen;

application Serial Number 08/397,809 entitled "LOOKASIDE BUFFER FOR ADDRESS TRANSLATION IN A COMPUTER SYSTEM" filed on March 3, 1995 by Leon Kuo-Liang Peng, Yolin Lih and Chih-Wei David Chang;

application Serial Number 08/397,893 entitled "RECLAMATION OF PROCESSOR RESOURCES IN A DATA PROCESSOR" filed on March 3, 1995 by Michael C. Shebanow, Gene W. Shen, Ravi Swami, Niteen Patkar;

application Serial Number 08/397,891 entitled "METHOD AND APPARATUS FOR SELECTING INSTRUCTIONS FROM ONES READY TO EXECUTE" filed on March 3, 1995 by Michael C. Shebanow, John Gmuender, Michael A. Simone, John R.F.S. Szeto, Takumi Maruyama and DeForest W. Tovey;

application Serial Number 08/397,911 entitled "HARDWARE SUPPORT FOR FAST SOFTWARE EMULATION OF UNIMPLEMENTED INSTRUCTIONS" filed on March 3, 1995 by Shalesh Thusoo, Farnad Sajjadian, Jaspal Kohli, and Niteen Patkar;

application Serial Number 08/398,284 entitled "METHOD AND APPARATUS FOR ACCELERATING CONTROL TRANSFER RETURNS" filed on March 3, 1995 by Akiro Katsuno, Sunil Savkar and Michael C. Shebanow;

application Serial Number 08/398,066 entitled "METHODS FOR UPDATING FETCH PROGRAM COUNTER" filed on March 3, 1995 by Akira Katsuno, Niteen A. Patkar, Sunil Savkar and Michael C. Shebanow;

application Serial Number 08/397,910 entitled "METHOD AND APPARATUS FOR PRIORITIZING AND HANDLING ERRORS IN A COMPUTER SYSTEM" filed on March 3, 1995 by Chih-Wei David Chang, Joel Fredrick Boney and Jaspal Kohli;

application Serial Number 08/398,151 entitled "METHOD AND APPARATUS FOR RAPID EXECUTION OF CONTROL TRANSFER INSTRUCTIONS" filed on March 3, 1995 by Sunil W. Savkar;

application Serial Number 08/397,800 entitled "METHOD AND APPARATUS FOR GENERATING A ZERO BIT STATUS FLAG IN A MICROPROCESSOR" filed on March 3, 1995 by Michael Simone;

application Serial Number 08/397,912 entitled "ECC PROTECTED MEMORY ORGANIZATION WITH PIPELINED READ-MODIFY-WRITE ACCESS" filed on March 3, 1995 by Chien Chen and Yizhi Lu; and

application Serial Number 08/398,299 entitled "PROCESSOR STRUCTURE AND METHOD FOR TRACKING INSTRUCTION STATUS TO MAINTAIN PRECISE STATE" filed on March 3, 1995 by Chien Chen, John R.F.S. Szeto, Niteen A. Patkar, Michael C. Shebanow, Hideki Osone, Takumi Maruyama and Michael A. Simone;

each of the above applications are incorporated herein by reference in their entirety.

Background of the Invention

Conventional digital addressable memory systems are subject to errors on both the data lines and the address lines. Errors may be caused by transients on the data and address lines on a memory card, as well as by other sources.

Error detection and correction codes, such as Hamming codes may be used to preserve data integrity. Information regarding Hamming and other codes may be found in Rao, T.R.N. & E. Fujiwara, *Error-Control Coding for Computer Systems, Prentice Hall Series in Computer Engineering* (Prentice-Hall, 1989).

Briefly, conventional Hamming theory conceptualizes the bits in each word to represent a vector, where the number of dimensions of the vector is equal to the number of bits in the word. Without the Hamming error code, each nearest pair of vectors is separated by no more than one unit, for example 00 is one unit from 01. The Hamming theory adds additional bits to the word, thereby allowing a greater space to represent the same number of vectors. For example, the data 01 may be mapped to the Hamming Code 00111 and data 00 may be mapped to the Hamming Code 00000, providing a three bit separation between the two binary data numbers. If one of the bits in the Hamming code is erroneously inverted, the resulting vector is corrected by adjusting it to equal the nearest vector. If two of the bits in the number are erroneously inverted, the error is detectible, though not properly correctible.

The number of bits which differ between the two nearest vector pairs is called the Hamming distance. Where d is the Hamming distance, the number of bit errors correctible is (d-1)/2 and the number of bit errors detectible is d-1.

While storing the Hamming code preserves the integrity of the data, the address remains susceptible to corruption, resulting in the storage or retrieval of potentially valid data from the wrong memory address. Conventional memory circuits include parity circuitry to help ensure address integrity by generating and sending a parity bit on the address lines, and checking the parity bit as close to the memory chips as possible. However, it is undesirable to have parity checkers immediately adjacent to each memory chip for cost and space reasons.

Thus, the above address parity error detection approach remains susceptible to address errors which may be induced in

the circuitry between the parity checkers and the memory chips. Such errors may lead to address errors without detection by the parity checkers.

Another approach stores the address parity bit along with the Hamming code. When the data is read from a target address, the parity bit is read and compared with the parity of the target address to detect single bit address errors. However, this approach is undesirable because of the increased cost and space required to store the extra bit.

Summary of Invention

In accordance with the present invention, a method and apparatus encodes the address parity into the stored data, providing address parity storage without requiring additional storage space or cost. When the data is read, only valid encoded parity bits are removed from the data, leaving invalid parity codes in the data to appear as errors. Because parity is stored with the data, even addressing errors which occur inside the memory chip are detectible.

Brief Description of the Drawings

Figure 1 is a block schematic diagram of an apparatus which encodes the address parity bit into a Hamming Code for storage in an addressable memory device according to one embodiment of the present invention.

Figure 2 is a block schematic diagram of an apparatus which removes only valid address parity bit from, and detects errors in, several bits of a stored Hamming code upon retrieval from an addressable memory device according to one embodiment of the present invention.

Figure 3 is a flowchart illustrating a method of encoding the address parity bit into a set of data bits and removing a valid encoded address parity bit from several data bits according to one embodiment of the present invention.

Detailed Description of a Preferred Embodiment

Referring now to Figure 1, a device **101** is shown which accepts data at inputs **102** and addresses at inputs **104**, generates a Hamming code and address parity, and encodes the address parity bit into two Hamming code bits. Conventional Hamming code generator **110** produces a Hamming Code containing bits **126, 128** and remaining bits **113** from data **112** to be stored. Conventional parity generator **115** generates a parity bit **117** from the memory address bits **114**. The parity generator **115** may generate conventional even parity, conventional odd parity, or any other code to distinguish one set of addresses from another set. Exclusive-OR gates **122, 124** encode the address parity bit **117** from parity generator **115** into two bits **120** of the Hamming Code **113** for writing into the memory at the indicated address **104**.

In one embodiment, two EXCLUSIVE-OR gates **122, 124** encode the address parity bit **117** onto any two bits **126, 128** of the Hamming Code **113**, although the parity bit **117** may be encoded into any number of Hamming Code bits. When the address parity bit is encoded into a number of data bits greater than the detectible number of erroneous bits the detection device is made simpler as described below. For example, a double bit error detection, single bit error correction code uses two EXCLUSIVE-OR gates **122, 124** as shown in Figure 1.

The encoded bits **130, 132** and the remaining bits of the Hamming Code **134** are output at data outputs **136** to be stored in a memory device at the address indicated by address outputs **138**. The two parity encoded Hamming bits **130, 132** replace the two original Hamming Code bits **126, 128**, respectively for storage.

Referring now to Figure 2, an apparatus for detecting address errors and non-correctible Hamming errors in data read from a memory device is shown. An address from which to read the data is input at address input **208**. Conventional parity generator **210** generates parity of the address to be read, and provides an input **212, 214** to each of the EXCLUSIVE-OR gates **216, 218**. As described above, parity generator **210** may generate

conventional even parity, conventional odd parity, or any other scheme. Data stored as described above is read from memory device **234** and output onto lines **220, 222, 228**. Hamming code bits **220, 222** onto which parity was encoded as described above are placed on lines **220, 228**, and provide the second input to each EXCLUSIVE-OR gate **216, 218**. The output **240, 242** of the EXCLUSIVE-OR gates **216, 218** are substituted in place of data bits on lines **220, 222** and, along with the remaining Hamming code bits **228** are input into conventional Hamming error detector **230** which asserts output **232** if a non-correctible error is detected. If, as described above, the parity is encoded into a number of bits greater than the correctible number of bits, and at least as large as the detectible number of bits, detection of single bit address errors may be accomplished at the same time and using the same apparatus to test non-correctible data errors.

Referring now to Figure **3**, one embodiment of the method of the present invention is shown. Parity is generated from an address and an error code is generated from the data **308**. In one embodiment, odd parity is generated **308**. In another embodiment, even parity is generated **308**. In another embodiment, both even and odd parity is generated **308**. Any other similar method for generating a one bit or larger identifier for the address may also be used as a parity. In one embodiment, a Hamming code is generated as the error code **308**. In another embodiment, a data parity bit is appended to the data in order to generate the error code **308**. In another embodiment, no transformation is made the error code generated is equal to the data **308**.

At least one bit is selected from the error code as the selected bits **310**. In one embodiment, the number of selected bits is equal to the non-correctible number of bits of the Hamming code. The parity is hashed into the error code by exclusive-or-ing the parity bit and the selected bits of the error code, and substituting the result in place of the selected bits of the error code **312, 314**. The resulting error code is stored in an addressable storage device such as a RAM memory array **316**.

The stored error code is retrieved using a target address, and address parity is generated **318**. The parity stored in the selected bits is unhashed by exclusive-or-ing the parity generated in step **318** with the selected bits to produce an unhashed error code **320**. The error code is decoded **322** and then checked for errors **324**. An error in the error code in at least as many bits as were selected may indicate an addressing error, and if fewer errors are detected, addressing errors may not have occurred **324, 326, 328**.

In one embodiment, a Hamming code is used as the error code and a number greater or equal to the non correctible number of bits is used as the number of selected bits. This allows checking for addressing errors to be performed at the same time the data is checked for errors. A number of errors greater or equal to the hamming distance indicates bad data or improperly addressed data, allowing common error detection circuitry to be used to reject data which may have had errors on addressing lines during storage or retrieval.

What is claimed is:

1. An apparatus for encoding address verification information into a plurality of data bits comprising a first set and a second set, the apparatus comprising:

a first input for accepting a plurality of address bits;

a parity generator having an input coupled to the first apparatus input and an output equal to the parity of the parity generator input;

a second input for accepting the plurality of data bits;

an encoder having a first input coupled to the parity generator output, a set of second inputs coupled to receive the first set of data bits, the encoder for encoding the parity bit into the first set of data bits and presenting at a set of encoder outputs the set of parity bit encoded data bits; and

a set of outputs coupled to a plurality of encoder outputs.

2. The apparatus of claim 1 wherein the encoder comprises a plurality of exclusive-or gates, each having a first input coupled to the first encoder input, a second input coupled to one of the set of second encoder inputs, and an output coupled to one of the set of encoder outputs.

3. The apparatus of claim 3 wherein the number of encoder exclusive or gates is at least as great as a non correctible Hamming number of the data bits.

4. The apparatus of claim 1 wherein the parity generator output is odd parity of the parity generator input.

5. The apparatus of claim 1 wherein the parity generator output is even parity of the parity generator input.

6. An apparatus for detecting addressing errors from a plurality of data bits stored in an addressable memory device having a plurality of address inputs and plurality of outputs, the apparatus comprising:

a plurality of address inputs coupled to receive a set of address bits and coupled to the addressable memory device address inputs;

a plurality of data inputs comprising a first set and a second set, the plurality of data inputs coupled to a plurality of the memory device plurality of outputs;

a parity generator having a set of inputs coupled to the address inputs and an output equal to the parity of the set of inputs;

a number of exclusive-or gates, each having a first input coupled to the parity generator output, a second input coupled to one of the first set of data inputs, and an output equal to the exclusive or of the first input and the second input; and

an error detector having a set of at least one input coupled to the output of at least one of the number exclusive-or gate outputs, and an output having a first state if the error detector detects an error condition and a second state if the error detector does not detect an error condition.

7. The apparatus of claim 6 wherein the error detector is a Hamming code error detector and the error condition occurs when the error detector input receives an invalid Hamming code.

8. The apparatus of claim 7 wherein the error condition occurs when the error detector input receives a non-correctible invalid Hamming code.

9. The apparatus of claim 6 wherein the parity generator generates even parity.

10. The apparatus of claim 6 wherein the parity generator generates odd parity.

11. A method of detecting errors in addressing a plurality of data bits, comprising the steps of:

generating a first parity of a first address;

encoding the first parity generated into a first number of at least one of the data bits;

storing the parity-encoded data bits;

using a second address to retrieve a second set of data bits;

generating a second parity of the second address;

decoding the second parity from a second number of at least one of the second set of data bits;

testing at least one of the decoded second set of data bits; and

responsive to the decoded second set of data bits having a value in a first set of values, indicating an error has occurred.

12. The method of claim 11 comprising the additional step of responsive to the decoded second set of data bits having a value in a second set of values, indicating no error has occurred.

13. The method of claim 11 wherein the first address is equal to the second address.

14. The method of claim 11 wherein the testing step comprises checking the decoded second set of data bits for a valid Hamming code.

15. The method of claim 11 wherein the first number comprises at least a non-correctible Hamming number of the first set of data bits.

16. The method of claim 11 wherein the second number is equal to the first number.

17. The method of claim 11 wherein the encoding step comprises exclusive-or-ing the first parity with at least one of the first set of data bits.

18. The method of claim 11 wherein the decoding step comprises exclusive-oring the second parity with at least one of the second set of data bits.

19. The method of claim 11 wherein the generating steps comprise generating even parity.

20. The method of claim 11 wherein the generating steps comprise generating odd parity.

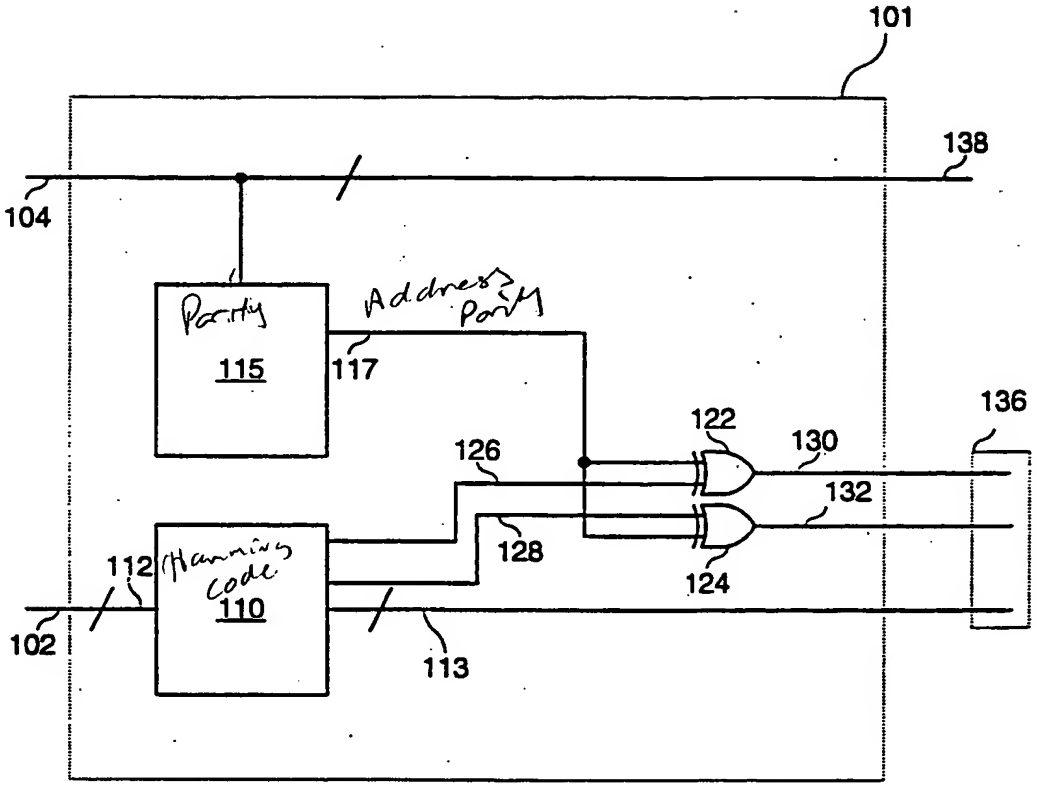
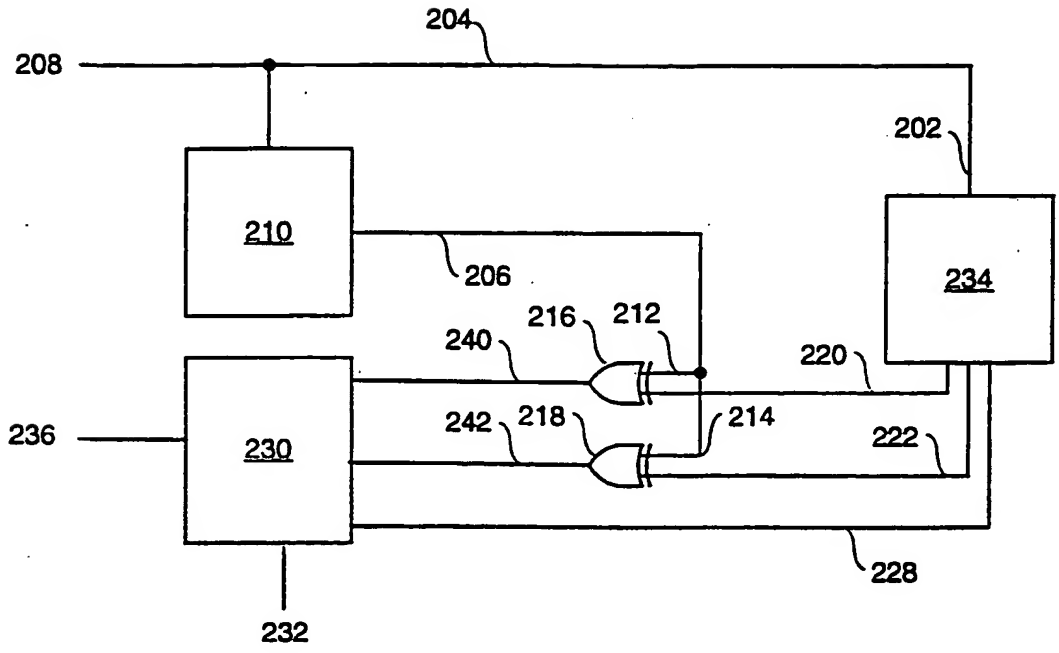

101
138
104
Parity
115
117
Address Parity
122
130
136
126
132
128
124
112
Hamming code
110
102
113

Fig. 1


204
208
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206
234
216
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236
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228
232

Fig. 2

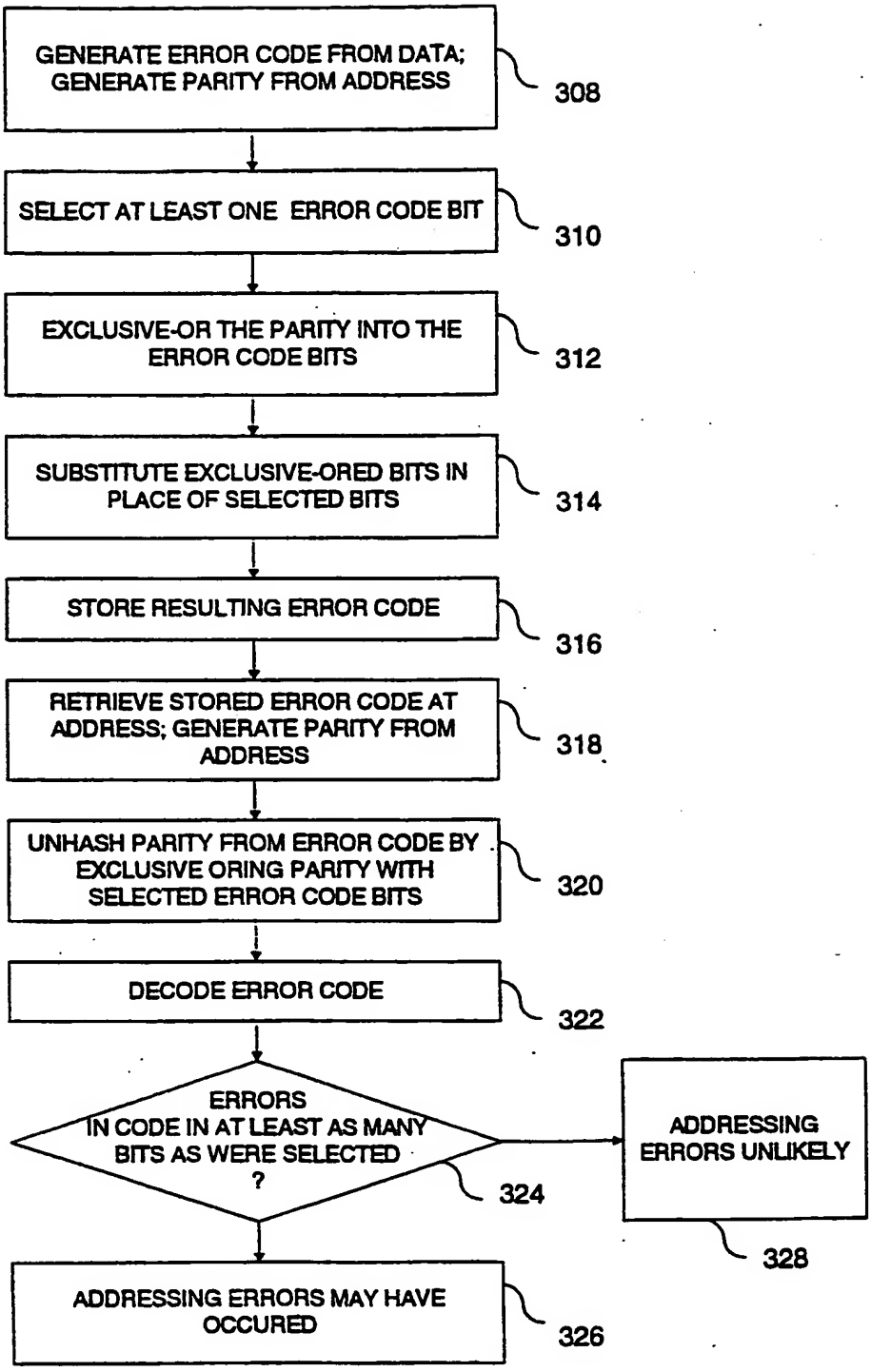
GENERATE ERROR CODE FROM DATA; GENERATE PARITY FROM ADDRESS
308
SELECT AT LEAST ONE ERROR CODE BIT
310
EXCLUSIVE-OR THE PARITY INTO THE ERROR CODE BITS
312
SUBSTITUTE EXCLUSIVE-ORED BITS IN PLACE OF SELECTED BITS
314
STORE RESULTING ERROR CODE
316
RETRIEVE STORED ERROR CODE AT ADDRESS; GENERATE PARITY FROM ADDRESS
318
UNHASH PARITY FROM ERROR CODE BY EXCLUSIVE ORING PARITY WITH SELECTED ERROR CODE BITS
320
DECODE ERROR CODE
322
ERRORS IN CODE IN AT LEAST AS MANY BITS AS WERE SELECTED ?
324
ADDRESSING ERRORS UNLIKELY
328
ADDRESSING ERRORS MAY HAVE OCCURED
326

Fig. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 96/09635

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F11/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE,A,26 55 653 (SIEMENS AG) 22 June 1978 see the whole document	1-20
X	EP,A,0 084 460 (TANDEM COMPUTERS INCORPORATED) 27 July 1983 see the whole document	1-20
A	US,A,5 345 582 (TSUCHIYA) 6 September 1994	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 96/09635

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE-A-2655653	22-06-78	NONE	
EP-A-84460	27-07-83	AU-B- 558156	22-01-87
		AU-A- 1138183	23-08-84
		CA-A- 1203027	08-04-86
		GB-A,B 2114335	17-08-83
		JP-C- 1739151	26-02-93
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		JP-A- 58171798	08-10-83
		US-A- 4672609	09-06-87
US-A-5345582	06-09-94	NONE	